In the Claims

Claims 1-31 (cancelled)

32. (previously amended) A capacitor construction comprising a first capacitor electrode over a substrate, a capacitor dielectric layer over the first electrode, a second capacitor electrode over the dielectric layer, and an atomic layer deposited insulative barrier layer to oxygen diffusion between the first and second electrodes.

33. (previously amended) The construction of claim 32 wherein the barrier layer has a thickness of less than about 12 Angstroms.

34. (previously amended) The construction of claim 32 wherein the barrier layer comprises Al_2O_3.

35. (previously amended) The construction of claim 32 wherein the barrier layer exhibits a K factor of greater than about 7 at 20° C.

D1

36. (currently amended) A capacitor construction comprising:

a first capacitor electrode over a substrate;

an insulative barrier layer to oxygen diffusion over the first electrode, the barrier layer comprising a chemisorption product of first and second substantially saturated precursor monolayers;

a capacitor dielectric layer over the first electrode; and

a second capacitor electrode over the dielectric layer and the barrier layer.

37. (previously amended) The construction of claim 36 wherein the barrier layer has a thickness of less than about 12 Angstroms.

38. (previously amended) The construction of claim 36 wherein the barrier layer comprises Al_2O_3.

39. (previously amended) The construction of claim 36 wherein the barrier layer exhibits a K factor of greater than about 7 at 20° C.

40. (previously added) A memory array comprising:

a plurality of capacitor constructions each having a first capacitor electrode over a substrate, a capacitor dielectric layer over the first electrode, a second capacitor electrode over the dielectric layer, and an atomic layer deposited insulative barrier layer to oxygen diffusion between the first and second electrodes.

41. (previously added) The array of claim 40 wherein the barrier layer has a thickness of less than about 12 Angstroms.

42. (previously added) The array of claim 40 wherein the barrier layer comprises Al_2O_3.

43. (previously added) The array of claim 40 wherein the barrier layer exhibits a K factor of greater than about 7 at 20° C.

D2

44. (currently amended) The array of claim 40 wherein the barrier layer comprises a chemisorption product of first and second substantially saturated precursor ~~layers~~ monolayers.

45. (previously added) A plurality of memory dice, each die comprising:

a section of a monocrystalline semiconductor wafer; and

a capacitor construction comprising a first capacitor electrode over the wafer, a capacitor dielectric layer over the first electrode, a second capacitor electrode over the dielectric layer, and an atomic layer deposited insulative barrier layer to oxygen diffusion between the first and second electrodes.

46. (previously added) The dice of claim 45 wherein the barrier layer has a thickness of less than about 12 Angstroms.

47. (previously added) The dice of claim 45 wherein the barrier layer comprises Al_2O_3.

48. (previously added) The dice of claim 45 wherein the barrier layer exhibits a K factor of greater than about 7 at 20° C.

D3

49. (currently amended) The dice of claim 45 wherein the barrier layer comprises a chemisorption product of first and second substantially saturated precursor ~~layers~~ monolayers.

50. (currently amended) The array of claim ~~40~~ 44 wherein the ~~barrier layer comprises a chemisorption product of~~ first and second ~~precursor monolayers~~ precursors are different.

51. (currently amended) The dice of claim ~~45~~ 49 wherein the ~~barrier layer comprises a chemisorption product of~~ first and second ~~precursor monolayers~~ precursors are different.

D4

52. (new) The construction of claim 36 wherein the first and second precursors are different.